REMARKS/ARGUMENTS

The non-final Office Action of October 5, 2004, has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested. Claims 1-2 and 9-11 have been amended. Claims 3-8 and 13-20 have been canceled. Claims 21-29 have been added. Claims 1-2, 9-12, and 21-29 remain pending.

Applicant has amended the specification to correct two minor typographical problems. These amendments do not add new matter and are fully supported by the Figures.

Responsive to the comments of the Examiner with respect to Figure 1, Applicant has amended Figure 1 to designate a legend of "(Prior Art)". Further, Applicant has amended a typographical error with respect to Figure 3. No new matter has been added for these amendments and support can be found within the original written description. Replacement and Annotated Sheets are attached as the Appendix herein.

Claim 1 has been amended to include many of the features of canceled dependent claim 7. New claim 26 includes many of the features of canceled dependent claim 8. Claims 21-24 include many of the features recited in dependent claims 9-12. New claim 27 includes many of the features recited in dependent claim 2. Claims 2, 9, 10, and 11 have been amended to correct claim dependency and/or minor typographical errors. Support for new claims 21-29 can be found throughout the original written description and drawings.

Claims 1-11 and 13-19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Frisch et al. (U.S. Patent No. 5,644,261, hereinafter referred to as *Frisch*). Applicant respectfully traverses this rejection.

Applicant's amended claim 1 recites, among other features,

> wherein when the output signal of the particular signal delay element is inverted vis-à-vis the signal (IN), the gate connected with the particular signal delay element is designed such that the gate advances the output signal in an inverted manner and, when the output signal of the particular signal delay element is non-inverted vis-à-vis the signal (IN), the gate connected with the particular signal delay element is designed such that the gate advances the output signal in a non-inverted manner.

Amendments to the Drawings:

The attached sheets of drawings include changes to Figures 1 and 3. These sheets, which include Figures 1, 3, and 4, replace the current sheets including Figures 1, 3, and 4. The amendments correct minor typographical errors as noted in the attached annotated sheets showing changes.

Attachment: Replacement Sheets
Annotated Sheets Showing Changes

The Action asserts that *Frisch* describes each and every feature of Applicant's independent claim 1. Contrary to the Action's assertion, *Frisch* fails to teach or suggest at least this feature of Applicants' independent claim 1.

The Action cites Figure 6 of *Frisch* and elements of the *Frisch* system that allegedly correlate to features of Applicant's claim 1. The Action allegedly correlates Applicant's "plurality of signal delay elements" to delay elements 76 of *Frisch* of which three are shown (see Action, page 2), and Applicant's "gate" correlates to the switch/gate 34 of *Frisch* (see Action, page 3). Further, the Action allegedly correlates Applicant's "particular signal delay element" to the first left inverter 76 of *Frisch* (see Action, page 3).

Applicant's feature of claim 1 recited above includes that when the output signal of the particular signal delay element is inverted vis-à-vis the signal (IN), the gate connected with the particular signal delay element is designed such that the gate advances the output signal in an inverted manner. If applied to the *Frisch* system, when the output signal of the first left inverter 76 is inverted, the multiplexer 34 connected with the first left inverter 76 is connected through an additional inverter. Thus, the output of the switch 34 would be non-inverted. As such, the *Frisch* system fails to teach or suggest that the gate advances the output signal in an inverted manner. Similarly, the *Frisch* system fails to teach or suggest that the gate advances the output signal in a non-inverted manner when the output signal of the first left inverter 76 is non-inverted. Therefore, *Frisch* fails to teach or suggest each and every feature of Applicant's claim 1. As such, withdrawal of the rejection is respectfully requested.

Applicant's claims 2 and 21-25, which depend from claim 1, are patentably distinct over the art of record for at least the same reasons as their ultimate base claim and further in view of the novel features recited therein. For example, the art of record fails to teach of suggest that,

> wherein when the output signal of the particular signal delay element is inverted vis-à-vis the signal (IN), the gate connected with the particular signal delay element includes two n-channel field effect transistors and two p-channel field effect transistors, and when the output signal of the particular signal delay element is non-inverted vis-à-vis the signal (IN), the gate connected with the particular signal delay element includes one n-channel field effect transistor and one p-channel field effect transistor,

as recited, among other features, in Applicant's claim 25.

Applicant's amended claim 26 recites features similar to those recited in canceled dependent claim 8. Applicant's claim 26 recites many of the same features recited in Applicant's claim 1. For at least similar reasons to those recited above with respect to Applicant's claim 1, Applicant's claim 26 is patentably distinct over *Frisch*. The *Frisch* system fails to teach or suggest that the gate advances the output signal in an inverted manner. Similarly, the *Frisch* system fails to teach or suggest that the gate advances the output signal in a non-inverted manner when the output signal of the first left inverter 76 is inverted. Therefore, *Frisch* fails to teach or suggest each and every feature of Applicant's claim 26. As such, withdrawal of the rejection is respectfully requested.

Applicant's claims 9-12 and 27-28, which depend from claim 26, are patentably distinct over the art of record for at least the same reasons as their ultimate base claim and further in view of the novel features recited therein. For example, the art of record fails to teach of suggest that,

> wherein when the output signal of the particular signal delay element is inverted vis-à-vis the signal (IN), the gate connected with the particular signal delay element includes one n-channel field effect transistor and one p-channel field effect transistor, and when the output signal of the particular signal delay element is non-inverted vis-à-vis the signal (IN), the gate connected with the particular signal delay element includes two n-channel field effect transistors and two p-channel field effect transistors,

as recited, among other features, in Applicant's claim 28.

Claims 12 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Frisch* in view of Nii (U.S. Patent No. 6,624,667, hereinafter referred to as *Nii*). Applicant respectfully traverses this rejection.

Applicant's dependent claims 12 and 24 each include the feature, "wherein at least one of the inverter circuit arrangements is a tristate inverter circuit arrangement." Claim 12 and 24 depend on independent claims 26 and 1 respectively. *Nii* fails to cure the deficiencies of *Frisch* as described above with reference to claims 1 and 26. As such, Applicant's dependent claims 12 and 24 are patentably distinct over the combination of *Frisch* and *Nii* for at least the same reasons as their ultimate base claim.

Applicant's new independent claim 29 recites, among other features,

a second gate, connected to the output of the second signal delay element, configured to output the delayed signal when the second gate is activated, the second gate including one p-channel field effect transistor and one n-channel field effect transistor, the drains of the one n-channel field effect transistor and the one p-channel field effect transistor connected with the other and with the output of the second gate, and the sources of the one n-channel field effect transistor and the one p-channel field effect transistor connected with the other and with the input of the second gate.

This feature of Applicant's independent claim 29 is neither taught nor suggested by *Frisch*, either alone or in combination with *Nii*. As such, Applicant's claim 29 is patentably distinct over the art of record.

CONCLUSION

All rejections having been addressed, Applicant respectfully submits that the instant application is in condition for allowance, and respectfully solicits prompt notification of the same. Should the Examiner find that a telephonic or personal interview would expedite passage to issue of the present application, the Examiner is encouraged to contact the undersigned attorney at the telephone number indicated below. If any additional required fees are or if an overpayment has been made the Commissioner is authorized to charge or credit Deposit Account No. 19-0733. Applicant looks forward to passage to issue of the present application at the earliest convenience of the Office.

Respectfully submitted,
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Date: January 5, 2005

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Replacement Sheets

Annotated Sheets Showing Changes

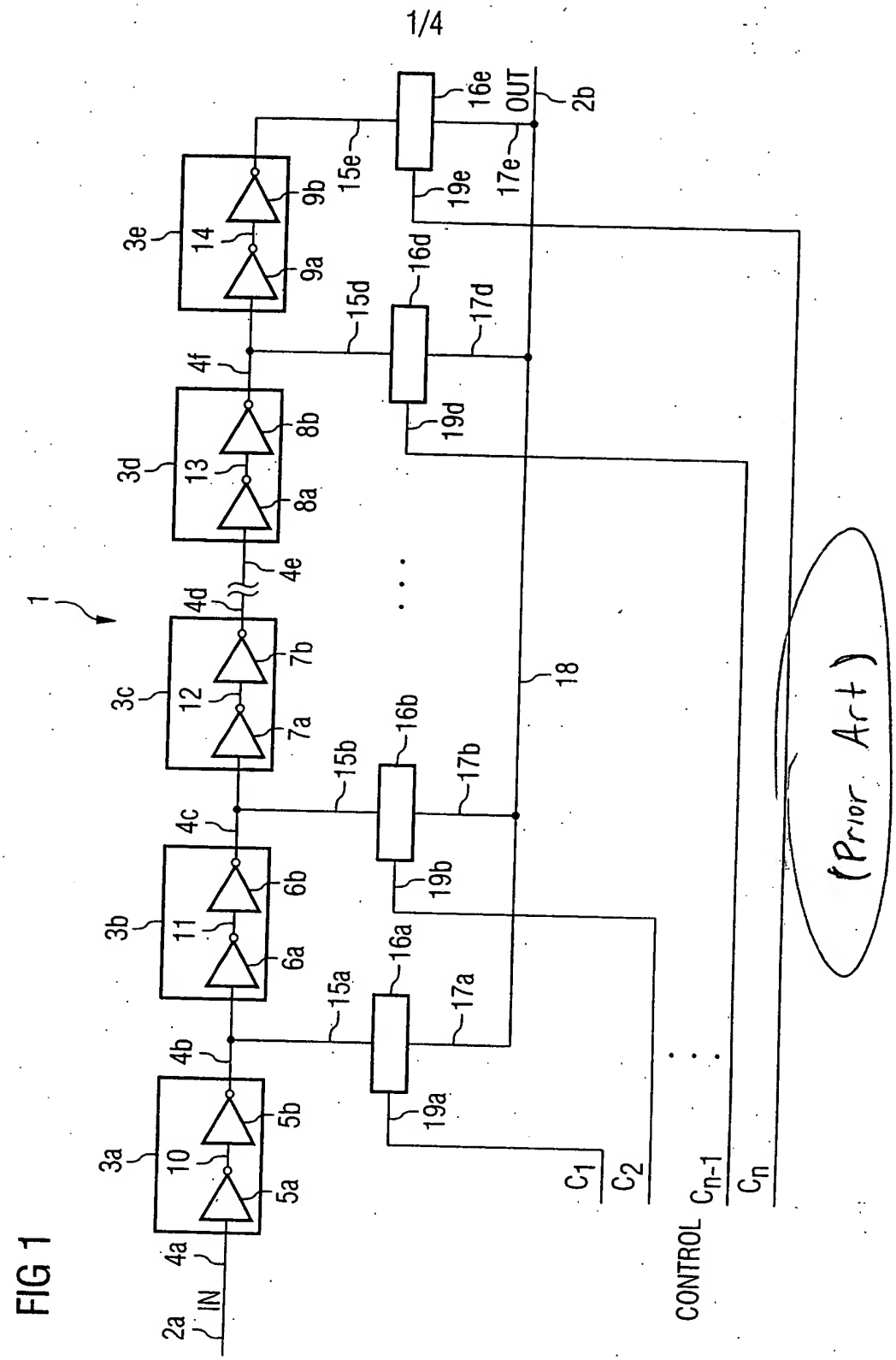
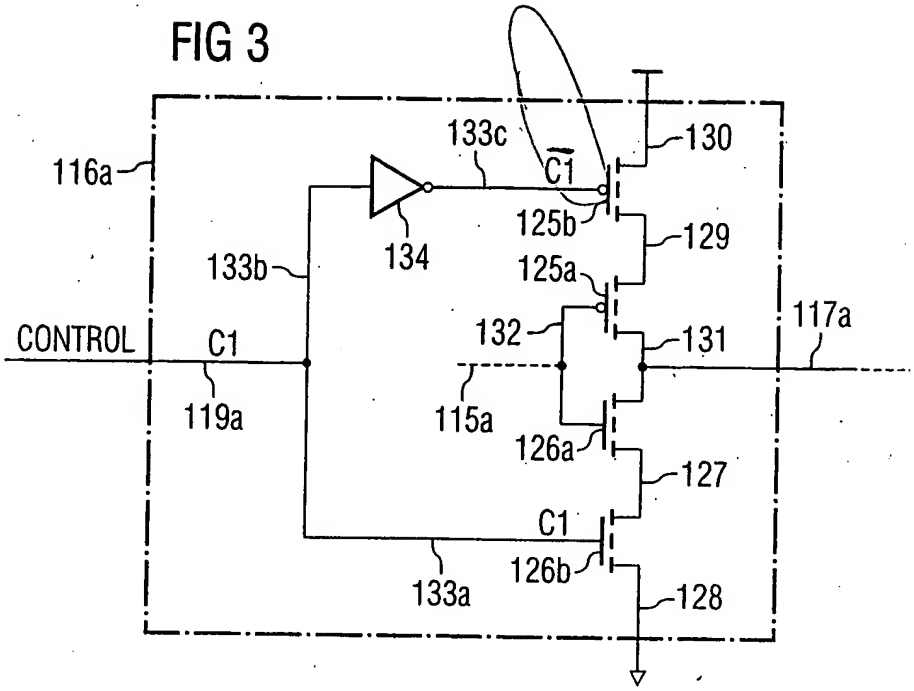


FIG 1

FIG 3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C1
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133a
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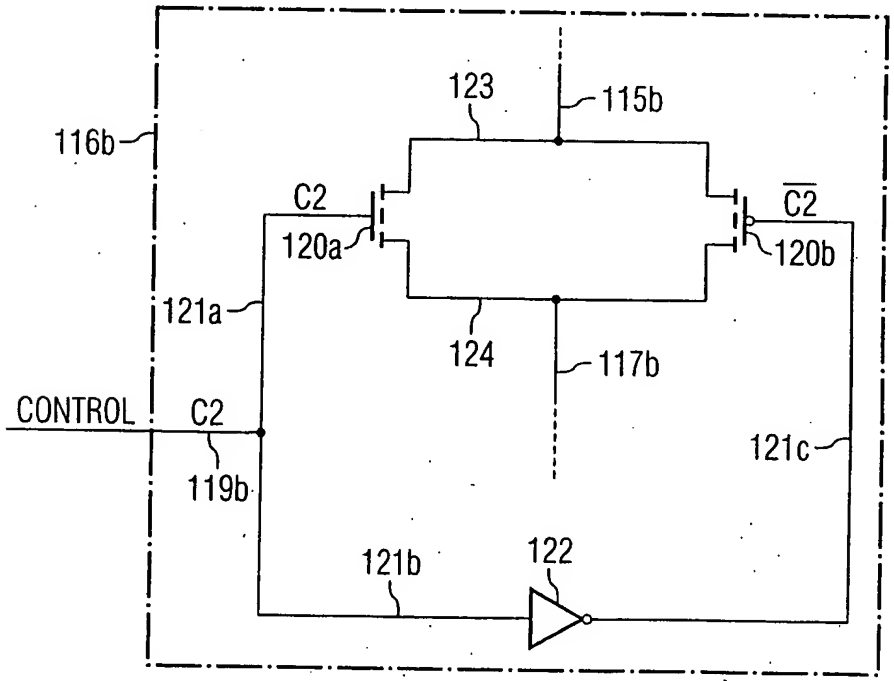
FIG 4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CONTROL
C2
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122